LISTING OF CLAIMS

1-67: (Cancelled.)

68.(Previously Presented) A memory comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;

wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

69.(Previously Presented) A memory as claimed in claim 68, wherein said first group of memory cells and said second group of memory cells are accessible by a common sector address.

70.(Previously Presented) A memory as claimed in claim 68, further comprising an erasing circuit to erase data stored in at least one or more of said plurality of memory cells in response to an erasing signal.

71.(Previously Presented) A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;

wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of

said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.

72.(Previously Presented) The memory as claimed in claim 71, further comprising an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal.

73.(Previously Presented) The memory as claimed in claim 71, wherein said first group of memory cells and said second group of memory cells are accessed by a common sector address.

74.(Previously Presented) A memory comprising:

a plurality of memory cell blocks further comprising;

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.

75.(Previously Presented) The memory as claimed in claim 69, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.

76.(Previously Presented) The memory as claimed in claim 73, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.

77.(Previously Presented) The memory as claimed in claim 74, wherein said first group of memory cells and said second group of memory cells are accessed by a common sector address.

78.(Previously Presented) The memory as claimed in claim 77, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.